PerfectVIPs
Right Tools... Perfect Chip

HIGHSPEED USB 2.0 VIP

DATASHEET
Rev. 2b

GENIE-USB

USB 2.0 HIGH SPEED VERIFICATION IP

OVERVIEW

The Genie-USB Verification IP Products are the industry's most advanced verification solution for USB 2.0 based designs. The intelligent **Verification Engine** provides a Bus Functional Model (BFM) for stimulus generation, error injection, protocol checking and an extensive list of callbacks. A unique **Interface Inspector** provides the monitoring, checking, and scoreboarding capability along with protocol compliance, functional coverage and error reporting. A comprehensive **Compliance Suite** is available with test cases for complete verification. This provides the Perfect combination of tools to ensure design success.

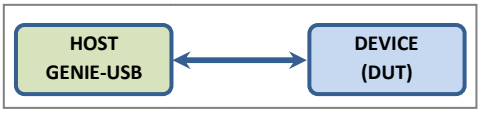

Fig. 1: Example Device Design Verification

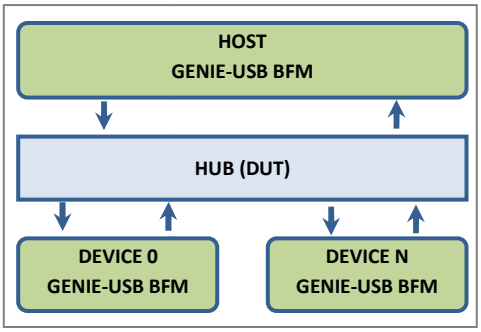

Fig. 2: Example Hub Design Verification

The **Genie-USB VIP** provides a quick and efficient way to verify any USB 2.0 based design – Host, Device or PHY. It supports the USB 2.0 specification. It tests all layers of the USB design – PHY, Link and Protocol. Genie-USB provides a complete verification solution that includes multi-language support and UVM and OVM methodology.

The Genie-SSU VIP provides:

- Bus Functional Models
- Protocol Checker
- Protocol Monitor
- Scoreboard
- Report Generator
- Error Injector
- Extensive Functional Coverage
- Callback Capability

FEATURES

❖ Complete Functional USB 2.0 Verification - Host, Device & PHY	❖ Compliant to USB 2.0 and 1.1 specifications
❖ Operates at High Speed USB rate of 480 Mbps	❖ Supports UTMI, D+/- and ULPI interfaces
❖ Direct access to configuration, reset, power, and state registers	❖ Supports all USB transactions: Control, Isochronous, Interrupt, and Bulk
❖ Automatic handling of Protocol, Link and PHY layer packets	❖ Automatic /user configurable generation of flow control packets
❖ Supports Link Power Management	❖ Configurable packet size for data packet payloads
❖ System level and block level testing	❖ Configurable for 0 to n endpoints
❖ Multiple Language Interface – SystemVerilog and Verilog	❖ Supports randomization for all BFM Knobs and error injections
❖ Comprehensive Compliance Suite	❖ Supports UVM and OVM

BENEFITS

❖ Guarantees compliance to USB 2.0 specifications	❖ Enable faster testbench development and complete USB design verification
❖ Plug-and-play into all major simulation environments	❖ Ensure first pass design success
❖ Reduces risk to design flaws	❖ Reduces overall design and verification costs

VMMenabled UVM OVM

PRODUCT DETAILS

USB Host

The Genie-USB Host VIP provides a Bus Functional Model (BFM) that operates at 480 Mbps. The BFM initiates data transfer cycles and emulates the interface. The programmable Error Injector permits errors to be inserted at any layer of the protocol.

- Host performs bus enumeration and allocates independent USB pipes for communication flow
- Program TP sequences for Bulk, Isochronous, Interrupt, and Control transfer types USB Device

USB Device

The Genie-USB Device BFM responds to data transfers from the host DUT according to the USB 2.0 device specification. Multiple instantiations of the device model can be configured in the simulation environment.

- Program USB Device requests to access USB device descriptors
- Support from 0 to N endpoints – each endpoint programmed separately
- Supports automatic response to all transaction types
- User configurable flow control

USB PHY

Integrated into the Host and Device BFM, the USB PHY model provides accurate modelling of the UTMI, ULPI and the D+/- interface.

- Connect to RTL (MAC) on UTMI/ULPI and PHY on D+/- side

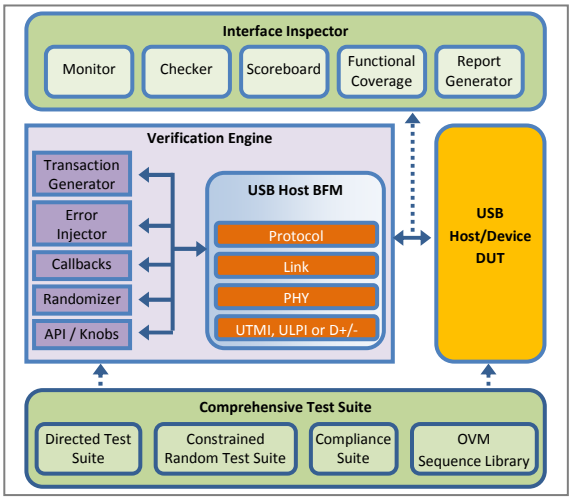

Fig. 3: USB Verification Environment

USB Interface Inspector

An enhanced protocol checker and monitor with built in coverage features; it can be integrated into any USB 2.0 verification environment, between upstream and downstream ports.

- Checks for protocol compliance and flags violations
- Generates bus performance summary and transaction statistics
- Performs functional/feature/error/protocol compliance coverage

USB 2.0 COMPLIANCE SUITE

Developed by PerfectVIPs to thoroughly exercise USB 2.0 designs, the compliance suite:

- Verifies all layers of USB 2.0 designs
- Provides comprehensive design coverage targeted at Protocol, Link & PHY layers
- Unified customizable message formatting and reporting
- Inject error at all layers
- Pre-built cover groups for functional coverage analysis
- Powerful and flexible pre-built OVM sequence libraries for generating test scenarios for coverage driven verification
- Pre-built constraint library which allows constrained random stimulus generation ensuring robust verification
- Developed with actual customer designs

USB 2.0 SOLUTIONS

Developed by PerfectVIPs to address all USB 2.0 architectures, the following solutions are available:

Verification IP:

- USB 2.0 Host VIP
- USB 2.0 Device VIP
- USB 2.0 Interface Inspector

Compliance Suites:

- USB 2.0 Host Compliance Test Suite
- USB 2.0 Device Compliance Test Suite

Supported Simulators

- Aldec, Cadence, Mentor and Synopsys

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